37. (New) A microprocessor comprising:

a register storing a register value corresponding to a threshold temperature;

a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if a microprocessor temperature exceeds the threshold temperature corresponding to the register value;

clock circuitry for providing a clock signal for the microprocessor; and

a processor unit coupled to the clock circuitry, wherein the processor unit executes instructions to vary the frequency of the clock signal in response to the first interrupt signal.

38. (New) The microprocessor of claim 37 further comprising:

a fail-safe thermal sensor generating a fail-safe interrupt signal if the microprocessor temperature exceeds a fail-safe threshold temperature, wherein the processor unit is halted in response to the fail-safe interrupt signal.

39. (New) The microprocessor of claim 37 wherein the clock circuitry further comprises a phase locked loop.

40. (New) The microprocessor of claim 37 wherein the thermal sensor comprises:

a current source;

a voltage reference coupled to the current source to provide a bandgap reference voltage, wherein the bandgap reference voltage is substantially constant over a range of temperatures;

programmable circuitry providing an output voltage varying with the microprocessor temperature in accordance with the register value; and

a comparator, wherein the comparator generates the first interrupt signal if a difference between the output voltage and the bandgap reference voltage indicates that the threshold temperature has been exceeded.

41. (New) The microprocessor of claim 40 wherein the programmable circuitry further comprises:

a transistor coupled to the current source to provide the output voltage, a gain ratio of the output voltage to a junction voltage of the transistor controlled by a transistor bias, wherein the junction voltage varies in accordance with a junction temperature of the transistor, the junction temperature corresponding to the microprocessor temperature;

a bias circuit providing the transistor bias to control the gain ratio, wherein the output voltage varies with the microprocessor temperature in accordance with the register value.

42. (New) The microprocessor of claim 41 wherein the bias circuit further comprises binary weighted resistors.

43. (New) A computer system comprising:

an active cooling device;

a microprocessor comprising:

a register storing a register value corresponding to a threshold temperature;

a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if a microprocessor temperature exceeds the threshold temperature, wherein the active cooling device is activated in response to the interrupt signal.

44. (New) The computer system of claim 43 wherein the active cooling device comprises a fan.

45. (New) The computer system of claim 44 further comprising:

clock circuitry for providing a clock signal for the microprocessor, wherein a frequency of the clock signal is reduced in response to the first interrupt signal.

46. (New) The computer system of claim 45 wherein the clock circuitry further comprises:

a first clock;

a frequency divider coupled to the first clock to provide the clock signal, the frequency divider reducing a frequency of the clock signal in response to the interrupt signal; and

a second clock circuit coupled to provide the clock signal to the microprocessor.

47. (New) The computer system of claim 46 wherein the microprocessor further comprises:

a processor unit coupled to the second clock circuit, wherein the processor unit executes instructions to vary the frequency of the clock signal from the second clock circuit in response to the first interrupt signal.

48. (New) The computer system of claim 47 wherein the processor unit programs the register with another register value corresponding to another threshold temperature in response to the first interrupt signal.

49. (New) A method of controlling a temperature of a microprocessor, wherein the microprocessor performs the steps of:

a) generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor;

b) comparing the temperature signal with a first threshold temperature level within the microprocessor;

c) generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded; and

d) decreasing a microprocessor clock frequency in response to the interrupt signal.

50. (New) The method of claim 49 further comprising the steps of:

e) comparing the temperature signal with a second threshold temperature level, wherein the second threshold temperature level represents a fail-safe temperature; and

f) halting the microprocessor, if the temperature signal indicates that the second threshold temperature level has been exceeded.

51. (New) A method of controlling a temperature of a microprocessor, wherein the microprocessor performs the steps of:

a) generating a temperature signal within the microprocessor corresponding to the temperature of the microprocessor;

b) comparing the temperature signal with a first threshold temperature level within the microprocessor;

c) generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded; and

d) activating an active cooling device to decrease the microprocessor temperature in response to the interrupt.

52. (New) The method of claim 51 wherein the active cooling device is a fan.

53. (New) The method of claim 51 further comprising the steps of:

e) comparing the temperature signal with a second threshold temperature level, wherein the second threshold temperature level represents a fail-safe temperature;

f) halting the microprocessor if the temperature signal indicates that the second threshold temperature level has been exceeded.

54. (New) A method of controlling a frequency of a clock signal which drives a microprocessor, comprising the steps of:

a) generating a temperature signal within the microprocessor corresponding to a temperature of the microprocessor;

b) generating a first threshold signal if the temperature signal indicates that the microprocessor temperature exceeds a first threshold temperature;

c) generating a second threshold signal if the temperature signal indicates that the microprocessor temperature exceeds a second threshold temperature; and

d) varying a frequency of the clock signal in response to at least one of the first and second threshold signals.

55. (New) The method of claim 54 further comprising the step of programming the first and second predetermined threshold levels within a programmable register.

56. (New) The method of claim 54 wherein step d) further comprises the step of decreasing the frequency of the clock signal if the first threshold signal is asserted.

57. (New) The method of claim 54 wherein step d) further comprises the step of increasing the frequency of the clock signal if neither the first threshold signal nor the second threshold signal are asserted.

58. (New) The method of claim 54 wherein step d) further comprises the step of driving the clock signal at an intermediate frequency if the second threshold signal is asserted and the first threshold signal is deasserted.

59. (New) A microprocessor comprising:

a processor unit;

a clock circuit providing a clock signal to the processor unit, the clock signal having an associated frequency;

a thermal sensor generating a temperature signal corresponding to a temperature of the microprocessor;

logic circuitry coupled to the thermal sensor, the logic circuitry generating a first signal if the temperature signal exceeds a first threshold level and a second signal if the temperature signal exceeds a second threshold level; and

means for varying the associated frequency of the clock signal in response to at least one of the first and second signals.

60. (New) The microprocessor of claim 59 further comprising at least one programmable register for storing a first threshold value corresponding to the first threshold level.